REMARKS

Claims 1-16 and 18-21 are pending in this application, of which claims 1 and 2 have been amended. Claim 17 has been cancelled. Claims 11-16 and 18 have been withdrawn from consideration. Claims 19-21 are newly-added.

Claims 1-10 and 17 stand rejected under 35 USC §112, second paragraph, as indefinite.

Accordingly, claim 1 has been amended to correct the noted instance of indefiniteness, and the 35 USC §112, second paragraph, rejection of claims 1-10, as amended, should be withdrawn.

The Examiner has indicated that claims 1-10 would be allowable if amended to overcome the 35 USC §112, second paragraph, rejection.

In view of the aforementioned amendments and accompanying remarks, claims 1-10, as amended as well as newly-added claims 19-21 are in condition for allowance, which action, at an early date, is requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Version with markings to show changes made
Substitute Abstract of the Disclosure

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/855,590

IN THE ABSTRACT:

Amend the Abstract as follows:

In a semiconductor device having a multiple layer wiring structure, a wiring method, a wiring device, and a recording medium, by optimizing the placement of SVIA, it is possible, for an intersection portion where a lower metal wiring layer having a width W1 and an upper metal wiring layer having a width W4 intersect with the intermediate metal layers sandwiched in between, to delete one row in the X direction and two rows in the Y direction for a total of nine SVIAs, when five SVIAs are arranged at the pitch PX in the X direction (i.e., in the transverse direction of the upper metal wiring layer) and three SVIAs are arranged at the pitch PY in the Y direction (i.e., in the transverse direction of the lower metal wiring layer) for a total of fifteen SVIAs. As a result, it is possible to secure one wiring track through which wiring is able to pass from among the three wiring tracks in the X direction and two wiring tracks through which wiring is able to pass from among the five wiring tracks in the Y direction.

IN THE SPECIFICATION:

Amend the specification as follows:

Paragraph beginning at page 10, line 6 has been amended as follows:

An embodiment shown in Fig. 2 shows an example of [when the present invention is applied] an intersection portion 10 in which the lower metal wiring layer M1 having [the] a width W1 and [the] an upper metal wiring layer M4 having [the] a width W4 intersect with the intermediate metal layers M2 and M3 sandwiched in between. In this example, SVIA that have been placed in an array configuration matching the wiring tracks in the priority wiring direction of the intermediate metal layers M2 and M3 over the entire surface of the intersection portion 10 are deleted in line units.

Paragraph beginning at page 10, line 22 has been amended as follows:

Specifically, an example is given of when it is possible to delete one row in the X direction and two rows in the Y direction for a total of nine SVIAs, when five rows of SVIA are arranged at the pitch PX in the X direction (i.e., in the transverse direction of the upper metal wiring layer M4) and three rows of SVIA are arranged at the pitch PY in the Y direction (i.e., in the transverse direction of the lower metal wiring layer M1) for a total of fifteen SVIAs. As a result, it is possible to secure one wiring track L3 through which wiring is able to pass from among the three wiring tracks T3 in the X direction and two wiring tracks L2 through which wiring is able to pass from among the five wiring tracks T2 in the Y direction.

IN THE CLAIMS:

Cancel claim 17.

Please amend claims 1 and 2 as follows:

1. (Amended) A semiconductor device having a multiple layer wiring structure that is provided with two or more metal layers and having a stack VIA portion in which, when connecting in a connection area a connection metal layer and a layer to be connected that is removed from the connection metal layer with one or more intermediate metal layers, [the intermediate metal layers are connected in sequence starting from the intermediate metal layer adjacent to the connection metal layer,] wherein

the semiconductor device having a multiple layer wiring structure [is provided with] comprises:

two or more partitioned intermediate metal layers that are partitioned [the intermediate metal layer] inside the connection area; and

an intermediate metal layer wiring area that is sandwiched by the partitioned intermediate metal layers.

2. (Amended) The semiconductor device [having a multiple layer wiring structure] according to claim 1, wherein [the connection area is an intersection portion where] the connection metal layer and the layer to be connected intersect in a connection area.